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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,276	04/12/2001	Roger Lewis	H26651	4922

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EXAMINER	
SHAPIRO, LEONID	
ART UNIT	**PAPER NUMBER**
2673	5

DATE MAILED: 05/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/834,276	LEWIS, ROGER	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Election/Restrictions

1. Claims 13,20 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 3

Drawings

2. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to because in Fig. 10, item 918 called "CLOCK". It should be change to the 'TIMER', as in specification on Page 11, Lines 16-17. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-6, 8-9,11-12,14-17,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuraski et al. (US Patent No. 5,589,805).

As to claim 1, Zuraski et al. teaches a method for pulse width modulation comprising the steps of: providing a pulse width modulator having n (6) bits of resolution (See Figs. 1A-B, 3, items Tc,T1,T2,17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8) and nominal time period Pn (Tpwm) (See Figs. 1A-B, 3, items Tpwm, 17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8); supplying an additional timer to generate K (2) associated states and having period Pt (T1 or T2) (See Fig. 3,1A-B, items T1, T2, 17, in description See Col. 5, Lines 9-27); associating a modulator output value with each one of K states (See Figs. 1A-B, 3, items Tc,T1,T2,17, in description See Col. 5, Lines 9-27).

Zuraski et al. does not show establishing a pulse width modulation update interval K*Pt. Zuraski et al. shows Tc= 2*T1 in his method to improve PMW system resolution. It would have been obvious to one of ordinary skill in the art at the time of the invention to multiply number of the states of the counter by the period of the resolution to obtain the update rate in order to enhance the output resolution of PWM system as an obvious variation in a method to improve PWM system resolution (See Col. 1, Lines 34-46 in the Zuraski et al. reference).

As to claim 5, Zuraski et al. teaches a method for improving the resolution of an n (6) bit pulse width modulator (See Figs. 1A-B, 3, items Tpwm,17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8) having a nominal time period Pn (Tpwm) (See Figs. 1A, 3, items Tc, 17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8), comprising the steps of : supplying an additional timer having K (2) associated states and timer period Pt (T1 or T2) (See Fig. 3,1A-B, items

T1,T2, 17, in description See Col.5, Lines 9-27); associating a modulator output value with each one of K states (See Figs. 1A-B, 3, items Tc,T1,T2,17, in description See Col. 5, Lines 9-27).

Zuraski et al. does not show outputting a pulse according to modulator output value during each time period Pn occurring within timer period Pt during each one of K timer states, whereby the resolution of n bit pulse width modulator substantially equals n+ log2 (K). Zuraski et al. shows 2 to the power of 6 equal 64 discrete pulse width modulation states (See Fig. 1B, in description See Col. 5, Lines 1-5) to improve PMW system resolution. It would have been obvious to one of ordinary skill in the art at the time of the invention to comply with the formula 1 + log2 (2) in the Zuraski et al. method in order to enhance the output resolution of PWM system as an obvious variation in a method to improve PWM system resolution (See Col. 1, Lines 34-46 in the Zuraski et al. reference).

As to claims 11-12, Zuraski et al. teaches a computer program product for pulse width modulation comprising: a computer readable storage medium having computer readable program code embedded in medium (See Figs. 3-5, items 10, 501-509, in description See Col. 7, Lines 5-20), computer readable program code means having: a first computer instruction means for associating K timer states a period Pt (See Fig. 5, items 507-509, in description See from Col. 7, Line 300 to Col. 8, Line 10); a second computer instruction means for reading a commanded pulse width modulation cycle (See Fig. 5, item 501, in description See Col. 7, Lines 22-30); a third computer instruction means for assigning a n bit modulator output with each one of K states according to the duty cycle (See Figs. 5-6, items 503, 601, in description See Col. 8, Lines 12-29).

As to claims 14, 19, Zuraski et al. teaches an apparatus for pulse width modulation comprising n (6) bit pulse width modulator (See Figs. 1A-B, 3, items Tc,T1,T2,17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8) having nominal time period Pn (Tpwm) (See Figs. 1A-B, 3, items Tpwm, 17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8); a timer to generate K (2) associated states and having period Pt (T1 or T2) (See Fig. 3,1A-B, items T1, T2, 17, in description See Col. 5, Lines 9-27); a computing device for assigning a modulator output value to each of K states (See Figs. 5-6, items 503, 601, in description See Col. 8, Lines 12-29).

Zuraski et al. does not show modulator outputs a plurality of pulses according to modulator output value during each Pn period occurring within timer period Pt and whereby pulse width modulator has a resolution of n+log2 (K). Zuraski et al. shows 2 to the power of 6 equal 64 discrete pulse width modulation states (See Fig. 1B, in description See Col. 5, Lines 1-5) to improve PMW system resolution. It would have been obvious to one of ordinary skill in the art at the time of the invention to comply with the formula 6 + 1 in the Zuraski et al. method in order to enhance the output resolution of PWM system as an obvious variation in a method to improve PWM system resolution (See Col. 1, Lines 34-46 in the Zuraski et al. reference).

As to claims 2,6,16, Zuraski et al. teaches Pt is an integer multiple of Pn, since Tc and Tpwm are both derived from microprocessor clock (See Fig. 3, item 17, in description See Col. 3, Lines 33-40).

As to claims 4,8 Zuraski et al. teaches conventional case where Pt=Pn (T1=Tpwm without internal microprocessor timers) (See Figs. 1A-B, 3, in description See Col. 5, Lines 9-27).

As to claims 9,17, Zuraski et al. teaches Pt (T1) >> Pn (Tpwm) (See Figs.1A-B, items Tpwm and Tc, T1, T2).

Zuraski et al. does not show Pt is other than integer multiple of Pn. It would have been obvious to one of ordinary skill in the art at the time of the invention to use external clock to the timers of the microprocessor to have Pt other than integer multiple of Pn in the Zuraski et al. method.

As to claim 15, Zuraski et al. teaches timers are included within computing device (See Fig. 3, item 10, in description See Col. 3, Lines 30-36).

5. Claims 3, 7, 10, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable Zuraski et al. as aforementioned in claims 1, 5, 14 in view of Shibuya et al. (US Patent No. 6,191,868 B10)

Zuraski et al. does not show pulse width modulator includes an overflow bit.

Shibuya et al. teaches to truncate the overflow bit (See Fig. 2, item 17, in description See Col. 4, Lines 58-65). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the overflow approach as shown by Shibuya et al. in the Zuraski et al. method and apparatus in order to enhance the output resolution of PWM system (See Col. 1, Lines 34-46 in the Zuraski et al. reference).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

The Miller et al. (US Patent no. 5,023,535) reference discloses high resolution pulse width modulation.

The Proffitt et al. (US Patent no. 6,138,047) reference discloses low frequency PWM generation method for a microprocessor-based controller

The Iwata et al. (US Patent no. 5,889,424) reference discloses pulse width modulation operation circuit.

The Akiko (JP No. 04-096417) reference discloses improvement of resolution of PWM by timer.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

ls
May 1, 2003

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